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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/031,326 02/26/98 KARNIEWICZ

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021186 TM02/0907  
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EXAMINER

PHAN, T

ART UNIT

PAPER NUMBER

2123

DATE MAILED:

09/07/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

# Office Action Summary

Application No.  
09/031,326

Applicant(s)  
Joseph J. Kat...wicz

Examiner  
Thal Phan

Art Unit  
2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on Jul 31, 2001
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☐ All b) ☐ Some\* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). \_\_\_\_\_
- 18) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

This Office Action is responsive to CPA application of 09/031,036. Claims 1-25 are pending in this official action.

1. Acknowledgment has been made for the drawings correction.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Robinson et al., patent no. 5,524,244.

As per claims 1 and 9, Robinson anticipated method, design system with databases stored in memory, program product for populating parameters of cells (Abstract, "Summary of the Invention", col. 3, line 65 to col. 5, line 30) for use in circuit design environment identical to the claimed invention. According to Robinson, the design apparatus includes global files for global variables and design data relating to layout and connectivity data of the functional block, a plurality of local files, each relating a plurality of local variables to the global variables (col. 6,

lines 21-36, col. 8, lines 41-67, col. 9, lines 1-12), and a plurality of cells, each cell corresponding to a local file and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the programmable cells (Figs. 3-12, cols. 50-56, 59-62 for example).

As per claims 2-3 and 10-11, Robinson disclosed local files include inherent file from source files, instance files, data files, etc. (Figs. 3-12).

As per claim 4, Robinson disclosed master files in hierarchical design acting as initial version of a corresponding local file for design, modification, increment compilation, .

As per claim 5, Robinson disclosed file or clean sheet file for containing design rules for a plurality of cells for coordinated design as claimed.

As per claim 6, Robinson disclosed file extraction and related variable extraction for design and update design.

As per claims 7-8, Robinson anticipated the design display in local host for display interactively interface.

As per claim 12, Robinson disclosed file update including update global file for coordinate process.

As per claim 13, Robinson anticipated local display in local user workstation for the design process.

As per claim 14, Robinson disclosed computer program in concurrent with design program for circuit design process as claimed.

As per claim 15, Robinson anticipates method and system of workstations, databases, shared memory, etc. for populating parameters of cells (Abstract, Figs. 3-12, cols. 4-5, 59-62, for example) for use in circuit design, programming design, etc. environment identical to the claimed invention. According to Robinson, the design apparatus includes local user work stations, central workstations, global files of global variables and design database, system memory for sharing between users (cols. 4, 5, col. 9, lines 12-23), a plurality of local files, each relating a plurality of local variables to the global variables (cols. 4-5, 50-56, 60-64, for example), and a plurality of instance cells being programmable, each cell corresponding to a local file and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the cells (Figs. 3-12, cols. 4-5, 50-56, 60-64, etc.) or updating variables in local file by reading from the global file value of global variables to which the local variables of the local file correspond as claimed.

Similarly, claims 16-21 are also rejected due to its similarities to claims 2-8 and claims 11-14.

As per claim 22, Robinson anticipated method, design system with databases stored in memory, program product for populating parameters of cells (Abstract, "Summary of the Invention", col. 3, line 65 to col. 5, line 30) for use in circuit design environment identical to the claimed invention. According to Robinson, the design apparatus includes global files for global variables and design data relating to layout and connectivity data of the functional block, a plurality of local files, each relating a plurality of local variables to the global variables (col. 6,

lines 21-36, col. 8, lines 41-67, col. 9, lines 1-12, cols. 50-56, 60-64, etc.), and a plurality of cells, each cell corresponding to a local file and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the programmable cells (Figs. 3-12, cols. 59-62 for example).

As per claims 23-24, Robinson anticipated inherent design file, and instance file in the design database.

As per claim 25, Robinson anticipated design framework for use in the chip design process. Such design framework could be used as CADENCE functional design system as claimed.

### ***Response to Arguments***

4. Applicant's arguments filed June 04, 2001 have been fully considered but they are moot in view of a new ground of rejection.

### ***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

(703) 308-9051, (for formal communications)

**Or:**

(703) 308-1396 (for informal or draft communications, please label

"PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,  
Arlington, VA., Sixth Floor (Receptionist).

September 5, 2001

  
KEVIN J. TESKA  
SUPERVISORY  
PATENT EXAMINER